EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	26192	((verif$5 check$4 simulat$4 synthes$6 violat$5 satisf$6) same (pld cpld pal pla fpla epld eepld lca fpga (programmable adj (gate logic) adj (array device))))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/14 18:12
L2	8943	l1 and ((partition$4 block allot distribut$4 divi$5 portion$3 segregat$3 split$4 section segment$3 size) with (chip ic die (integrated adj circuit) (pld cpld pal pla fpla epld eepld lca fpga (programmable adj (gate logic) adj (array device)))))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/14 18:13
L3	182	l2 and ((generat$4 determ$5 optim$6 resolv$3 ascertain$3 establis$3 produc$4 achiev$6 cause develop$4 initiat$3 make induce) with (rtl (register adj transfer adj language)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/14 18:15
L4	67	l3 and ((generat$4 determ$5 optim$6 resolv$3 ascertain$3 establis$3 produc$4 achiev$6 cause develop$4 initiat$3 make induce) with ((block near level) (block with (representation design schematic design))))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/14 18:16
L5	0	l4 and (rba ("ram" adj "bit" adj address))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/14 18:18
L6	0	(cram with (rba ("ram" adj "bit" adj address)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/14 18:20
L7	0	(configuration with (ram (random adj access adj memor$3))) with (rba ("ram" adj "bit" adj address))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/14 18:21

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L8	1	(configuration with (ram (random adj access adj memor$3))) same (rba ("ram" adj "bit" adj address))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/14 18:22
L9	438229	(full complete entire) with (chip ic circuit same3 design)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/14 18:24
L10	81644	l9 and ((partition$4 block allot distribut$4 divi$5 portion$3 segregat$3 split$4 section segment$3 size) with (chip ic die (integrated adj circuit) (pld cpld pal pla fpla epld eepld lca fpga (programmable adj (gate logic) adj (array device)))))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/14 18:25
L11	1216	l10 and (rtl (register adj transfer adj language))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/14 18:25
L12	148	l11 and ((configuration config) with (ram (random adj access adj memor$3)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/14 18:26
L13	0	l12 and ("rba" ("ram" adj "bit" adj "address"))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/14 18:28

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	18	(((config configuration) with (ram (random adj access adj memor$3))) or (eprom eeprom fuse (anti adj fuse) antifuse sram mram fram dram)) with (rba (ram adj bit adj address))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/14 19:00
L2	35	(((config configuration) with (ram (random adj access adj memor$3))) or (eprom eeprom fuse (anti adj fuse) antifuse sram mram fram dram)) same (rba (ram adj bit adj address))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/14 19:00
L3	5	l2 and (full complete entire) with (chip ic circuit same3 design)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/14 19:01
L4	6	l2 and ((partition$4 block allot distribut$4 divi$5 portion$3 segregat$3 split$4 section segment$3 size) with (chip ic die (integrated adj circuit) (pld cpld pal pla fpla epld eepld lca fpga (programmable adj (gate logic) adj (array device)))))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/14 19:02
L5	0	l4 and (rtl (register adj transfer adj language))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/14 19:03
L6	1	l2 and ((verif$5 check$4 simulat$4 synthes$6 violat$5 satisf$6) same (pld cpld pal pla fpla epld eepld lca fpga (programmable adj (gate logic) adj (array device))))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/14 19:04
L7	0	l4 and ((verif$5 check$4 simulat$4 synthes$6 violat$5 satisf$6) same (pld cpld pal pla fpla epld eepld lca fpga (programmable adj (gate logic) adj (array device))))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/14 19:04

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L14	0	(verif$7 and design and pld and partition$3 and "rtl" and ("rba" ("ram" adj "bit" adj address)) and (cram ((configuration config) with ("ram" (random adj access adj memor$3))))).clm.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/14 18:31